Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A circuit for detecting a logic transition comprising:

an input terminal receiving a logic signal;

an output terminal generating a detection signal;

a first capacitor;

a second capacitor;

an exchanging means for bringing the first capacitor from a first voltage to a second voltage and the second capacitor from the second voltage to the first voltage in response to a switching of the logic signal;

means for maintaining a command node at the first voltage in the steady condition;

means for generating a reset pulse through the first capacitor in response to the switching;

means for bringing the command node to the second voltage in response to the reset pulse;

a generator of current means for bringing back the command node to the first voltage through the second capacitor; and

logic means having a regulated threshold voltage comprised between the first and the second voltage, the logic means asserting the detection signal when the command node is brought to the second voltage and deasserting the detection signal when the command node reaches the threshold voltage.

2. (Original) The circuit according to claim 1 wherein the means for generating the reset pulse includes an electronic switch for connecting a reset node providing the reset pulse to the first capacitor.

3. (Original) The circuit according to claim 1 wherein the means for bringing the command node to the second voltage includes a further electronic switch for connecting the command node to a power supply terminal providing the second voltage in response to the reset pulse.

4. (Original) The circuit according to claim 1, further including means for enabling the current generator means in response to the detection signal.

5. (Original) The circuit according to claim 1, further including filtering means for filtering the logic signal.

6. (Original) The circuit according to claim 5, further including means for enabling the filtering means in response to the detection signal.

7. (Original) The circuit according to claim 1, further including connecting means for selectively connecting the command node to the second capacitor, and regulating means, having a further regulated threshold voltage, for enabling the connecting means when the command node is brought to the second voltage and for disabling the connecting means when the command node reaches the further threshold voltage.

8. (Original) The circuit according to claim 7 wherein the regulating means includes a logic gate controlling the transferring means, first biasing means of the logic gate for applying the regulated current provided by the current generator means and second biasing means of the logic gate for applying a further current higher than the regulated current, the first

biasing means being enabled when the detection signal is asserted and the second biasing means being enabled when the detection signal is deasserted.

9. (Original) An asynchronous memory device including a matrix of memory cells, means for receiving a selection address of the memory cells, the circuit according to claim 1 for detecting a switching of the address and means for enabling an operation on the memory cells selected by the address in response to the detection of the switching.

10. (Currently Amended) A circuit for detecting logic transition comprising:

an input terminal;

an output terminal;

a first logic circuit coupled to the input terminal, an output of the circuit first logic transitioning from a first logic level to a second logic level based on an input signal at the input terminal changing state;

a second logic circuit coupled to the input terminal, an output of the second logic circuit transitioning from the second logic level to the first logic level upon a signal at the input terminal changing state; and

a pulse generation circuit coupled to both the first logic circuit and the second logic circuit, an output of the pulse generation circuit having an initial logic level and changing logic levels upon the first or second logic circuits transitioning to different logic states and returning to the initial logic level after a selected period of time, the pulse generation circuit including a first capacitor.

11. (Canceled)

12. (Original) The circuit according to claim 11 wherein the pulse generation circuit includes a second capacitor and the voltage charge level of the first capacitor and the second capacitor change logic states each time an input signal applied at the input terminal changes logic states.

13. (Original) The circuit according to claim 10, further including an output drive circuit coupled to the pulse generation circuit which drives the output terminal.

14. (Original) The circuit according to claim 13 wherein the pulse generation circuit includes an inverter.

15. (Currently Amended) The pulse generation circuit according to claim 10 wherein the first ~~input~~ logic circuit includes an inverter.

16. (Original) A method of detecting a logic transition comprising:

maintaining a first capacitor and a second capacitor alternately at a first voltage and at a second voltage, respectively;

receiving an input logic signal;

maintaining a command node at the first voltage in the steady condition;

generating a reset pulse through the first capacitor in response to the switching;

bringing the command node to the second voltage in response to the reset pulse;

asserting the detection signal when the command node is brought to the second voltage;

bringing back the command node to the first voltage through the second capacitor using a generator of regulated current; and

deasserting the detection signal when the command node reaches a threshold voltage comprised between the first and the second voltage.

17. (Original) The method according to claim 16, further including temporarily driving an internal node from a first logic level to a second logic level and bringing the internal node back to the first logic level after a selected period of time.

18. (Original) The method according to claim 17 wherein the selected period of time is based on the charge rate of the first capacitor.